REMARKS

STATUS OF THE CLAIMS

In accordance with the foregoing, claims 1-5 have been amended. Claims 1-5 are pending and under consideration.

No new matter is being presented, and approval of the amended claims is respectfully requested.

NON-STATUTORY DOUBLE PATENTING

On page 2-3 of the Action, claims 1-5 are provisionally rejected under doctrine of non-statutory double patenting, as being unpatentable over claims 1-4 and 8 of co-pending Application No. 11/317,011.

A Terminal Disclaimer, in compliance with 37 CFR 1.321 is filed concurrently herewith. Thus, the non-statutory double patenting rejection is respectfully overcome and should be withdrawn. Of course, the enclosed Terminal Disclaimer does not provide for disclaiming in the event the other, co-pending, application does not issue into a patent.

REJECTIONS UNDER 35 U.S.C. §112

Claims 1-4 are rejected as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. Specifically, the Examiner points out that it is unclear how the recitations of the "device unit" relate to the "plurality of device units".

Claims 1-4 have been amended herein to further clarify the features recited therein and to maintain proper antecedent basis. As a result, it is respectfully submitted that the rejections under 35 U.S.C. §112 are overcome. Approval of the amended claims is respectfully requested.

REJECTIONS OF CLAIMS 1 AND 2 UNDER 35 U.S.C. §102(b) AS BEING ANTICIPATED BY OSAKA ET AL. (U.S. PATENT NO. 5,787,261)

The rejections of claims 1 and 2 are respectfully traversed and reconsideration is requested.

An object of the present invention of independent claim 1 is that when an active connection of a device unit is made, the influence of noise on another device unit or device connected to the same data bus is eliminated. As another object, the present invention prevents device units of a self system and other systems from malfunctioning when glitch noise that occurs in making an active-line connection or disconnection of a functional circuit board (device

unit), with respect to a data transfer bus (data bus), propagates to the device units.

That is, independent claim 1 relates to a timing design method in which the propagation of glitch noise occurring by active-line insertion, the time transition of a control signal of a bus switch, and the skew of a timing-signal are used as parameters. On the basis of these parameters, the timing at which glitch noise, occurring by active-line insertion, reaches device units of self and other systems is computed, thereby preventing a malfunction that occurs when these device units infringe a setup time at the time of synchronous operations.

On the other hand, Osaka et al. (hereinafter "Osaka") is directed to a method of enabling a functional circuit board to be connected and disconnected to and from a bus thereof, with signal lines remaining in an active state, without stopping or interrupting devices being operated and bus transfers in the devices. A second object of Osaka is to enable the functional circuit board to keep up with increased bus speeds, and to enable the functional circuit board to be inserted and withdrawn to and from a bus thereof with signal lines remaining in an active state without causing a malfunction to occur in other functional boards connected to the same bus.

Osaka discloses a functional circuit board equipped with a pre-charge resistor and a switching element connected in parallel to a connector at a location on an input/output signal path of the functional circuit in close proximity to the connector.

With this configuration, by connecting the switching element and pre-charge resistor in parallel, even if the functional circuit board is inserted in the connector with the switching element being off, no noise will occur on the bus. Even if the switching element is caused to be in an ON or conducting state after the insertion, noise on the bus can be minimized, because a difference in potential between the bus and the signal in the functional circuit has become sufficiently small by the action of the pre-charge resistor.

Finally, a third object of Osaka is to prevent the malfunction of a functional circuit board in another system.

Thus, Osaka describes an active-line inserting/withdrawing system in which the pre-charge resistor is connected in parallel with the switching element for performing clock synchronization control and in close proximity to a connector, and before electrically connecting the functional circuit board to a data transfer bus by operation of the switching element, a difference in potential between the data transfer bus and a signal path in the functional circuit board is minimized through the pre-charge resistor. Thereby, glitch noise that occurs at the time of active-line insertion is suppressed.

In contrast, independent claim 1 of the present application recites, computing noise propagation timing when each one of said plural device units is connected to said data bus

being active. Osaka, on the other hand, suppresses glitch noise that occurs at the time of active-line insertion by employing the pre-charge resistor.

In addition, in Osaka, to connect and withdraw a functional circuit board equipped with a functional circuit to and from a data transfer bus with signal lines remaining in an active state, it is disclosed that (i) on an input/output signal path of the functional circuit, a pre-charge resistor and a switching element connected in parallel are connected to a resistor in close proximity to the resistor; (ii) the pre-charge resistor is 200 to 1100 Ohms; (iii) in the case where the functional circuit board is inserted with signal lines remaining in an active state, after the connector has been completely connected and after the supply of power to the functional circuit board has been stabilized, the system resets the functional circuit, and switching control means controls the switching element from a non-conducting state to a conducting state; and (iv) there is provided switching control means by synchronizing the switching element with a delayed clock signal which delays a bus clock signal employed for data transfer by a time shorter than a bus-clock cycle time.

Thus, in Osaka, by preventing noise from occurring on the data transfer bus, when the functional circuit board is inserted in the data transfer bus with signal lines remaining in an active state, glitch noise is prevented from propagating to other functional circuit boards through the data transfer bus of a bus and causing malfunctions.

For example, Eq. (3) of Osaka shows an equation for minimizing glitch noise that occurs in inserting the functional circuit board with signal lines remaining in an active state. It is also disclosed that by arranging the pre-charge resistor near the switching element, and setting the value of the pre-charge resistor to a suitable value using Eq. (3) so that before the switching element is turned from OFF to ON, the potential of the input/output signal path of the functional circuit board to be inserted with signal lines remaining in an active state becomes close to the potential of the data transfer bus of the back panel, a capacitance terminal of another functional circuit board, that is a circuit input buffer potential, is not varied by glitch noise before and after the switching element is turned from OFF to ON.

In contrast, the present invention has the advantages of cost reduction and a reduction in the area of the circuit board, by not requiring the resistors required by Osaka, as well as the prevention of an increase in the stub wiring and capacity in an active-line connection place due to the installation of the pre-charge resistor, as required by Osaka.

A computer data bus, for example, to which embodiments of the present invention can be applied, generally has a great number of bits (such as 32 bits, 64 bits, etc.) and control signals, which, as taught by Osaka, would require a great number of resistors. However, the present

invention, as recited in independent claim 1, does not require such resistors.

The design method, according to claim 1, computes, for each of said plurality of device units, based on a cycle of said timing signal, a signal propagation delay in each one of said plurality of device units, signal propagation delays in said timing-signal bus and said data bus, and a setup time in another one of said plurality of device units or another device connected on said data bus, timing at which, when each one of said plurality of device units is connected on said data bus being active, noise propagates to the other one of said plurality of device units or to the other device connected on said data bus.

Therefore, embodiments of the present invention show the means for computing the timing at which glitch noise propagates to the device units of other systems connected to the data bus by active-line insertion.

Thus, the present invention is characterized in that glitch noise, which can occur by the active-line insertion/withdrawal of the device unit, is shifted intentionally from the timing of the device unit clock synchronizing operation. Therefore, the present invention is different from Osaka, which merely suppresses the occurrence of glitch noise by employing the pre-charge resistor.

Therefore, it is respectfully submitted that independent claim 1 patentably distinguishes over the cited art. Dependent claim 2 inherits the patentability of independent claim 1 and, thus, it is further submitted that claim 2 patentably distinguishes over the prior art for at least the reasons provided herein.

REJECTIONS UNDER 35 U.S.C. §103(a)

Claims 3-5 are rejected for obviousness as being unpatentable over Osaka. The rejections are respectfully traversed and reconsideration is requested.

Independent claims 4 and 5 recite similar features to those described above. Thus, the foregoing arguments are also submitted for independent claims 4 and 5.

Moreover, independent claims 4 and 5 further clarify that a timing margin M {= (T+g) – (a + b+c+d+e+f) – S} relative to a setup time S in a bus system is computed based on the period "T" of the clock of the data bus (timing signal), clock voltage skew "a" from the timing-signal supply source to the bus switch controller, a control delay time "b" from the input of a timing signal to the output of a bus switch control signal in the bus switch controller, a propagation delay time "c" of the bus switch control signal, an operation delay time "d" until the bus switch performs a connection operation from the reception of a control signal, a pulse width "e" of a flitch noise which occurs on a data bus when the bus switch is connected in a device unit that is

to be connected or withdrawn with signal lines remaining in an active state, a propagation delay time "f" during which the noise propagates to device units of a self system and other systems, skew "g" from the timing-signal supply source to each of the other device units, and a setup time "S" in the bus system. The control timing of the bus switch is determined so that the timing margin M is 0 or greater.

Furthermore, unlike Osaka, embodiments of the present invention show the time "f" during which glitch noise propagates to device units of other systems and the clock skew "g" of each of the device units, on the assumption that glitch noise occurs by the active-line insertion of the device unit into the data bus.

Therefore, it is respectfully submitted that independent claims 4 and 5 patentably distinguish over the prior art.

Dependent claim 3 depends from independent claims 1 and inherits the patentability thereof. Thus, it is further submitted that claim 3 also patentably distinguishes over the prior art.

CONCLUSION

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot. Further, all pending claims patentably distinguishes over the prior art. There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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